

**AMENDMENTS TO THE DRAWINGS:**

New formal drawings are attached as Replacement Sheets pages 1-36.

**REMARKS**

**I. Status of the Claims**

Claims 27, 28, and 30-33 are currently pending in this application. No claim has been amended.

**II. Drawings Objection**

At the outset, Applicants note that the Advisory Action does not indicate whether Applicants' Amendment After Final dated January 13, 2005, has been entered. That Amendment included new formal drawings in response to the Examiner's request for corrected drawings in the Final Office Action dated August 13, 2004. Applicants have resubmitted those drawings as drawing Replacement Sheets 1-36 herewith in order to insure that they be entered.

**III. Rejections Under 35 U.S.C. § 102(b)**

In the Final Office Action, the Examiner rejected claims 27, 28, and 30 to 33 under 35 U.S.C. § 102(b), as being anticipated by U.S. Patent No. 5,188,976 ("Kume et al.") for reasons discussed at page 3 of the Final Office Action. Applicants respectfully traverse the Examiner's rejection for the reasons set forth in Applicants' Amendment After Final and for the following reasons.

A rejection under § 102 is proper only when the claimed subject matter is identically described or disclosed in the prior art. *In re Arkley*, 455 F.2d 586, 587 (C.C.P.A. 1972). "For anticipation under 35 U.S.C. § 102, the reference must teach every aspect of the claimed invention either explicitly or impliedly." M.P.E.P. § 706.02.

Kume et al. does not anticipate the pending claims, because the reference fails to teach each and every element of the claim. Specifically, Kume et al. at least fails to

teach the claimed “side wall of the first gate electrode ... connected to a side wall of the second gate electrode above the isolation element when viewed from a direction perpendicular to the first direction,” as recited in claim 27.

In the Final Office Action, the Examiner asserts that FIG. 15 of Kume et al. shows a “side wall” of gate electrode 17 in a memory area which “is connected to side wall of second gate 17” in a first peripheral area in the drawing. See Office Action at 3. As stated in the Amendment After Final, Kume et al. teaches “film 17 is processed so as to have a shape suitable for the formation of a floating gate electrode.” (Emphasis added.) Col. 12, lines 50-53. Thus, film 17 in the memory area shown in FIG. 15 is surrounded by insulating material, and the side wall of film 17 in the memory area cannot form a connection with an adjacent film 17 in the first peripheral area, for example.

In the Advisory Action, the Examiner repeated his previous assertion that Kume et al. teaches “a sidewall of the first gate electrode is connected to a side wall of the second gate electrode.” Citing Fig. 15<sup>1</sup> and col. 12, lines 48-61 of Kume et al., the Examiner maintains that the sidewall of the first gate electrode 17 in the memory area is connected to the sidewall of the second gate electrode 17 in the first peripheral area. See Continuation Sheet of the Advisory Action.

Applicants respectfully disagree. Figs. 14 and 15 of Kume et al. show two consecutive intermediate steps of the manufacturing process disclosed therein. Fig. 14 shows the deposition of gate electrode 17 onto the memory transistor area and the first and second peripheral transistor areas. Fig. 15 shows the removal of the gate electrode

17 in the first and second peripheral transistor areas, leaving only gate electrode 17 in the memory transistor area. Figs. 14 and 15 clearly show, and col. 12, lines 48-61 describe, that in the memory transistor area, the gate electrode films 17 is surrounded by insulating film 18. Thus, the sidewall of the first gate electrodes 17 in the memory area and the sidewall of the second gate electrode 17 in the first peripheral area in Fig. 14 are clearly not connected. Accordingly, for this reason also, Kume et al. fails to teach the claimed "a side wall of the first gate electrode is connected to a side wall of the second gate electrode above the isolation element when viewed from a direction perpendicular to the first direction", as recited in claim 27.

Moreover, in the Advisory Action, the Examiner asserts that "Kume et al.'s Figs. 7, 9, 11 and 14 show #21 above isolation elements 18, 19 and 20 (which are over gate 17)." Figs. 7, 9, 11 and 14 of Kume et al., however, only show a single gate electrode 21, which is placed above gate electrode 17. Applicants are unclear as to what other gate electrode the sidewall of gate electrode 21 could be connected to.

In light of the above-described deficiencies of Kume et al., Applicants respectfully submit that claim 27 is allowable over the Kume et al. because it at least fails to teach the claimed "a side wall of the first gate electrode is connected to a side wall of the second gate electrode above the isolation element when viewed from a direction perpendicular to the first direction." Moreover, claims 28, and 30-33 are allowable at least due to their dependence from claim 27.

---

1 Applicants believe the Examiner was actually referring to Fig. 14 of Kume et al., because Fig. 15 shows only the first gate electrode 17 in the memory resistor area, and that the second gate electrode 17 in the first peripheral area has been removed.

In addition, with respect to claim 28, the Examiner asserts in the Advisory Action that in Kume et al., "the insulating films 18, 19 and 20 are perpendicular to 40 which is parallel to substrate 11, therefore, 18, 19 20 are perpendicular to surface of substrate 11." Applicants are unclear as to the basis for the Examiner's conclusions. According to Kume et al.'s Fig. 7, the insulating films 18, 19 and 20 are not perpendicular to the surface of substrate 11, but are parallel to it instead. Thus, claim 28 is allowable for this reason also.

**IV. Conclusion**

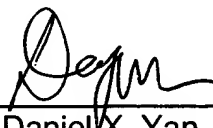
In view of the foregoing remarks, Applicants submit that this claimed invention is not anticipated by the prior art reference cited against this application. Applicants therefore request that the Examiner reconsider and reexamine the present application, and the timely issue a Notice of Allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account no. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,  
GARRETT & DUNNER, L.L.P.

Dated: April 14, 2005

By:   
Daniel X. Yan  
Reg. No. 54555

Attachment: Replacement Drawing Sheets pages 1 - 36.